

S-BUS protocol

Note- Much of this first page is from mbed, but it was written for the original s.bus using the "FASST MULT" mode. Here's the original page link-
<http://mbed.org/users/Digixx/notebook/futaba-s-bus-controlled-by-mbed/>

The protocol is 25 Byte long and is send every 14ms (analog mode) or 7ms (highspeed mode).
One Byte = 1 startbit + 8 databit + 1 paritybit + 2 stopbit (8E2), baudrate = 100'000 bit/s, **so one bit takes 10 microseconds.**

The highest bit is send first, so data "000000000001" = 1024

The logic is inverted out of the receiver.

[startbyte] [data1] [data2] [data22] [flags][endbyte]

startbyte = 11110000b (0xF0)

data 1-22 = [ch1, 11bit][ch2, 11bit] [ch16, 11bit] (ch# = 0 bis 2047)

channel 1 uses 8 bits from data1 and 3 bits from data2

channel 2 uses last 5 bits from data2 and 6 bits from data3

etc.

flags = bit7 = ch17 = digital channel (0x80)

bit6 = ch18 = digital channel (0x40)

bit5 = Frame lost, equivalent red LED on receiver (0x20)

bit4 = failsafe activated (0x10)

bit3 = n/a

bit2 = n/a

bit1 = n/a

bit0 = n/a

endbyte = 00000000b (**Prior to the s.bus2 capable receivers, and the R7003SB**)

The above info was decoded from the earlier s.bus receivers, before the R7008SB came out. The new receiver is sold with 18MZ and 14SG radios, and offers telemetry, as well as the ability to output PWM, s.bus, and s.bus2 at the same time. Unfortunately, it was immediately noted that none of the FC boards which previously supported s.bus worked with the new R7008SB.

Fortunately, not much changed in the protocol for the R7008SB. The original protocol above seems to be the same in the new R7008SB, with the exception of the endbyte. In the previous version, for example with the R6203SB receiver, the endbyte data was always 00000000. Now, the endbyte data seems to vary some.

"FASSTest 18CH" mode generates s.bus frames every 15ms. It allows 16 channels, plus two digital (on/off) channels, and all telemetry sensors to be used. Using "FASSTest 18CH" with the R7008SB, I've only captured the following 4 variations of endbyte data. I've tried everything I can think of to generate something different, but these are the only ones I can create. They appear in rotation in the order shown, which appears to form a two bit 0-3 counter (remembering that the high order bit is to the right).

```
00100000
00101000
00100100
00101100
```

"FASSTest 12CH" mode generates frames every 6.3ms. This only allows 10 channels, plus 2 digital (on/off) channels, and it only allows RX and Ext bat voltages for telemetry. For the "FASSTest 12CH" mode using the R7008SB, the protocol is the same, except the endbyte is fixed at 00010000. This would actually make an easy fix from the original s.bus code if you only wanted to use the FASSTest 12CH mode.

There's another brand new (about April 2013) receiver called the R7003SB. I assumed it wouldn't work with the old FC code either, but I was wrong :-). I've just captured the output, and it looks just like the older R6203SB. I just tested it on an OP board with the original s.bus code, and it works perfectly. This is very good news! The only reason not to use the R7003SB is in the case where you need more than 1-2 PWM channels directly from the receiver. Also, those channels have to be low, so if need to use a high channel number because your FC won't let you reassign (most will) then you would need the R7008SB.

Rusty

18MZ to R6203SB- "FASST MULTI" (all channels null)

(as captured)

```
1000011111001111111111001110111110001111110000001111111110010011111110011110111100
0111111101000111111111100110111111000111110111000111111110000111111111001110111110
0011111101100011111111110010111111100011110111100011111110100011111111100110111111
00011111011100011111111100001111111111001111111111
```

(inverted before FC input)

```
01111000001100000000001100010000011100000011111100000000001101100000001100001000011
100000001011100000000001100100000111000001000111000000001111000000000110001000001
11000000100111000000000011010000000111000010000111000000010111000000000011001000000
1110000010001110000000011110000000000110000000000
```

(inverted before FC input and grouped in 12 bit bytes)

011110000011 (Start byte)

00000000011 (data 1)

000100000111 CH1

000000111111 CH2

000000000011 CH3

011000000011 CH4

000010000111 CH5

000000010111 CH6

000000000011

001000000011 CH7

000001000111 CH8

000000001111

000000000011 CH9

000100000011 CH10

000000100111 CH11

000000000011

010000000011 CH12

000010000111 CH13

000000010111 CH14

000000000011

001000000011 CH15

000001000111 CH16

000000001111 (data 22)

000000000011 (flags byte) DCH1, DCH2, Frame lost, failsafe activated, rest are NA

000000000011 (11 added by dead space between frames)

18MZ to R6203SB -"FASST MULTI" (all channels null except ch1= 100%)

(inverted before FC input, difference from previous "all null" capture in red)

```
01111000001101111100101100110000001100000011111100000000001101100000001100001000011
10000000101110000000000110010000001110000010001110000000011110000000000110001000001
11000000100111000000000011010000000111000010000111000000010111000000000011001000000
1110000010001110000000011110000000000110000000000
```

(inverted before FC input, and grouped in 12 bit bytes)

011110000011 (Start byte)

011111001011 (data 1)

001100000011 CH1

000000111111 CH2

000000000111 CH3

011000000011 CH4

000010000111 CH5

000000101111 CH6

000000000111

001000000111 CH7

000001000111 CH8

000000011111

000000000111 CH9

000100000111 CH10

000000100111 CH11

000000000111

010000000111 CH12

000010000111 CH13

000000010111 CH14

000000000111

001000000111 CH15

000001000111 CH16

000000001111 (data 22)

000000000111 (flags byte) DCH1, DCH2, Frame lost, failsafe activated, rest are NA

0000000000 11 (11 added by dead space between frames)

18MZ to R7008SB - "FASSTest 18CH" (all channels null)

(as captured)

```
10000111110011111111111100111011111100011111100110010000000010011011111100011110111100
0111111101000111111111110011011111100011111011100011111110000111111111001110111110
00111111011000111111111110010111111100011110111100011111110100011111111100110111111
00011111011100011111111000011111111100111011111
```

(inverted as seen by FC)

```
0111100000110000000000110001000001110000001100110111111101100100000011100001000011
10000000101110000000000110010000001110000010001110000000011110000000000110001000001
11000000100111000000000011010000000111000010000111000000010111000000000011001000000
111000001000111000000001111000000000011000100000
```

(inverted as seen by FC)

011110000011 (Start byte)

00000000011 (data 1)

000100000111 CH1

00000010011 CH2

01111111011 CH3

001000000111 CH4

000010000111 CH5

00000010111 CH6

00000000011

001000000111 CH7

000001000111 CH8

00000000111

00000000011 CH9

000100000111 CH10

000000100111 CH11

00000000011

010000000111 CH12

000010000111 CH13

00000010111 CH14

00000000011

001000000111 CH15

000001000111 CH16

000000001111 (data 22)

00000000011 (flags byte) DCH1, DCH2, Frame lost, failsafe activated, rest are NA

(last byte cycles through these 4 versions in this order- added by dead space between frames)

000100000111

000101000011

000100100011

000101100111

18MZ to R7008SB - "FASSTest 12CH" (all channels null)

(as captured)

```
1000011111001111111111001110111110001111110110001111111110010011111110011110111100
011111110100011111111110011011111100011111011100011111110000111111111001110111110
0011111101100011111111110010111111100011110111100011111110100011111111100110111111
00011111011100011111111000011111111100111101111
```

(inverted as seen by FC)

```
01111000001100000000001100010000011100000010011100000000001101100000001100001000011
1000000010111000000000011001000000111000001000111000000001111000000000110001000001
11000000100111000000000011010000000111000010000111000000010111000000000011001000000
1110000010001110000000001111000000000011000010000
```

(inverted as seen by FC)

011110000011 (Start byte)

00000000011 (data 1)

00010000111 CH1

000000100111 CH2

00000000011 CH3

01100000011 CH4

00001000111 CH5

000000010111 CH6

00000000011

00100000011 CH7

000001000111 CH8

00000000111

00000000011 CH9

000100000111 CH10

000000100111 CH11

00000000011

010000000111 CH12

000010000111 CH13-NA

000000010111 CH14-NA

00000000011

001000000111 CH15-NA

000001000111 CH16-NA

00000000111 (data 22)

00000000011 (flags byte) DCH1, DCH2, Frame lost, failsafe activated, rest are NA

000010000111 (endbyte)

18MZ to R7003SB - "FASSTest 12CH" (all channels null)
18MZ to R7003SB - "FASSTest 18CH" (all channels null)
(both the same)

(as captured)

```
10000111110011111111110011101111100011111101100011111111110010011111110011110000000
0101101001100111111111100110111111000111110111000111111100001111111111001110111110
001111110110001111111110010111111000111101111000111111101000111111111100110111111
0001111101110001111111100001101111110001111111111
```

(inverted as seen by FC)

```
01111000001100000000001100010000011100000010011100000000001101100000001100001111111
1010010110011000000000011001000000111000001000111000000001111000000000110001000001
11000000100111000000000011010000000111000010000111000000010111000000000011001000000
1110000010001110000000011110010000001110000000000
```

(inverted as seen by FC)

011110000011 (start byte)

00000000011 (data 1)

000100000111 CH1

000000100111 CH2

000000000011 CH3

011000000011 CH4

000011111111 CH5

010010110011 CH6

000000000011

001000000011 CH7

000001000111 CH8

000000001111

000000000011 CH9

000100000011 CH10

000000100111 CH11

000000000011

010000000011 CH12

000010000011 CH13-NA

000000010111 CH14-NA

000000000011

001000000011 CH15-NA

000001000111 CH16-NA

000000001111 (data 22)

001000000011 (flags byte) DCH1, DCH2, Frame lost, failsafe activated, rest are NA

000000000011 (end byte)

